METHOD OF MANUFACTURING SEMICONDUCTOR ELEMENT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of manufacturing semiconductor element, especially, which has metallic silicide layer in its gate electrode.

2. Description of the Related Art

As high integration of semiconductor device proceeds, a demand for faster and finer element of semiconductor increases. To accept this demand, a gate electrode comprising metallic silicide layer is adopted for semiconductor element of MOS structure.

A gate electrode having metallic silicide layer is formed, for example, as described below.

At first, an isolation of an element is performed. After this, a gate oxide film and a polysilicon film are formed, in this order. Then, a metallic silicide layer is formed on the polysilicon film by PVD method or CVD method. And, a SiN layer is formed on the top of gate electrode with a thermal process using CVD of reduced pressure etc. This thermal process is performed at comparatively high temperature of a range of 700° C to 800° C.

After forming a SiN layer, a lithography for forming a gate electrode is performed. And, an etching for forming a gate electrode is performed with this patterned SiN layer used as a mask. Thus, a gate electrode is formed. And, after this, the photo-resist used for etching is removed.

After removing the photo-resist, oxide films are formed for covering

the side walls of the gate electrode with a CVD method of reduced pressure etc.

However, the conventional structure of gate electrode mentioned above could not sufficiently recover from the damage received during the etching process, for the side wall of gate electrode was covered with oxide film by a CVD method of reduced pressure. And, this is a problem to be solved. Moreover, over-etching of gate oxide film occurs. And, by this, it becomes impossible to compensate for thinning of gate oxide film. As a result, there was another problem of causing leak of gate.

Therefore, in order to prevent leak of gate, a method of performing heat oxidation treatment is generally used. But, in the method mentioned above, a heat treatment for forming SiN layer was necessary. Therefore, the metallic silicide was crystallized. And, the crystal was in a state that oxygen was likely to diffuse. An oxidation process in this state caused increasing oxidation of metal of W etc. and Si. And, expansion of volume occurred. Therefore, difference of stress occurred between polysilicon and metallic silicide in the lower portion of metallic silicide layer. And, difference of stress also occurred between metallic silicide and SiN layer in the upper portion of metallic silicide layer. As a result, fastening between metallic silicide layer and SiN deteriorated. And, peeling off of SiN layer occurred.

That is, according to the method mentioned above, a gate electrode 40 comprising polysilicon layer 42, metallic silicide layer 43,and SiN layer 44 was formed. And, when its surface was observed, the state of surface shown in Fig.5(b) was recognized. In Fig.5(b), metallic silicide crystal 45 grew like notches in the horizontal direction, because the side wall of gate electrode 40 was abnormally oxidized. And, SiN layer 44 was likely to peel off owing to abnormal oxidation as mentioned above.

As a method of preventing abnormal oxidation mentioned above, a method of implanting nitrogen in the side wall of gate electrode 40 has been suggested (c.f. JP 08-321613).

However, the conventional method has a problem that voids (vacancies) occurred because of nitrogen implanted in the semiconductor substrate.

SUMMARY OF THE INVENTION

Therefore, the present invention aimed at providing a method of manufacturing semiconductor substrate which can restrain occurrence of abnormal oxidation under heat treatment at high temperature after forming metallic silicide layer.

The problem mentioned above can be solved, because the present invention comprises as next.

The first is a method of manufacturing a semiconductor element comprising:

a process of forming gate electrode having metallic silicide layer on a semiconductor substrate,

a process of decreasing grain boundaries on the surface of the metallic silicide at least a portion of which is exposed, and

a process of forming spacer consisting of oxide film on the side wall of gate electrode.

The second is a method of manufacturing a semiconductor element according to the first method, wherein the process of decreasing said grain boundaries is a process of performing heat treatment to said metallic silicide layer in an atmosphere consisting of a chief element of nitrogen gas.

The third is a method of manufacturing a semiconductor element

according to the first method, wherein the process of decreasing said grain boundaries is a process of performing heat treatment to said metallic silicide layer in an atmosphere consisting of a chief element of argon gas.

The fourth is a method of manufacturing a semiconductor element according to the first method, wherein the process of decreasing said grain boundaries is a process of performing heat treatment to said metallic silicide layer in an atmosphere consisting of a mixture gas of chief elements of nitrogen and ammonia.

The fifth is a method of manufacturing a semiconductor element according to the first method, wherein the process of decreasing said grain boundaries is performed after performing a reduced pressure process.

These methods has a process of decreasing grain boundaries after forming metallic silicide layer. So, occurrence of abnormal oxidation in the side wall of gate electrode can be restrained, even if a process of treatment at high temperature is performed after the process of decreasing grain boundaries.

Here, the process of decreasing grain boundaries means a process of performing heat treatment to metallic silicide layer at least a portion of which is exposed in an atmosphere of inoxidizable gas consisted of a chief element of nitrogen, argon, or mixture gas of nitrogen and ammonia.

Moreover, for example, a chief element of nitrogen means an atmosphere including more than 99% density of nitrogen gas. Especially, it means a state of atmosphere including less than 100ppm of oxidizable gas (oxygen gas etc.). Incidentally, other inoxidizable gas can be included if the gas mentioned above is a chief element and the density of oxidizable gas is less than 100ppm.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a) to (d) are sectional views of semiconductor element in the process of an Embodiment of the present invention.

Fig. 2 is a plan view of the gate electrode formed by the method of present invention.

Fig. 3 is a sectional view of the gate electrode formed by the method of Embodiment 2 of present invention.

Fig. 4(a) and (b) are sectional views of NMOS-FET having LDD structure manufactured by the method of present invention.

Fig. 5(a) is a sectional view of a gate electrode formed by the conventional art, and (b) shows a state of abnormal oxidation of gate electrode.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereafter, Embodiments 1 to 4 of the method of manufacturing semiconductor element according to present invention will be described, referring to the drawings.

<Embodiment 1>

The Embodiment 1 of manufacturing method of present invention comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat treatment of said metallic silicide layer at least a portion of which is exposed, in a gas atmosphere consisting of a chief element of nitrogen (a heat treatment process of metallic silicide layer), and a process of forming spacers comprising oxide films on the side walls of said gate electrode; in this order.

In the concrete, at first, an isolation of an element is performed, as

shown in Fig. 1(a), by the method which is same as the conventional method known in public. After isolating an element, a gate oxide film 1 and a polysilicon layer 2 are formed, as shown in Fig. 1(b), by the method shown in public. Then, an ion implantation is performed so as to introduce impurity to the polysilicon layer 2 to make an electrode from it. And, a metallic silicide layer 3 is formed on the polysilicon layer 2 by PVD method or CVD method.. Here, the temperature for forming the metallic silicide layer 3 is preferably 400° C to 600° C. After forming the metallic silicide layer 3, a heat treatment which temperature is higher than that for forming the metallic silicide layer 3 is performed. Here, the temperature of this heat treatment is preferably 700° C to 800° C.

Incidentally, the way of heat treatment is not limited at all. However, the heat treatment can be performed together with a process of forming a SiN layer 4, which becomes a hard mask for forming gate and a mask for making self -aligned contact, on the top of the gate electrode.

In this occasion, the SiN layer 4 is preferably formed by CVD method of reduced pressure, which can make a minute film with little H included. The heat treatment by this CVD with reduced pressure is performed at a temperature higher than the temperature for forming the metallic silicide layer 3.

After forming the SiN layer 4, a photolithography for forming a gate electrode 5 is performed, as shown in Fig. 1(c). And, an etching for forming gate (process of forming gate electrode) is performed. By this gate etching, side walls of the portions of metallic silicide layer 3 are exposed.

After forming the gate electrode 5, it gets a heat treatment (process of heat treatment of metallic silicide layer) is performed. This is performed in a gas atmosphere including nitrogen as a chief element, in a chamber of heat

treating apparatus (RTA) purged with nitrogen for example.

The temperature of heat treatment in the heat treatment process of metallic silicide layer is preferably 700 to 800° C in a view point of decreasing grain boundaries of silicide crystal without fail. The process time is preferably 30 to 40 sec. in the same point of view.

Since the gas atmosphere in the chamber consists of a chief element of nitrogen, the gas atmosphere consists of little oxidizable gas. That is, the density of oxidizable gas in the atmosphere is less than 100 ppm. Therefore, diffusion of oxygen in the metallic silicide layer 3 is contained. And, abnormal oxidation can be prevented. Moreover, grain boundary of silicide crystal in the side wall becomes less. So, diffusion of oxygen or moisture after forming gate can be prevented.

Moreover, nitrogen gas is convenient for manufacturing devices, because it is not expensive and easy to use.

After performing heat treatment in the process of treating metallic silicide layer with heat, an oxidizing treatment is performed in a common furnace. By performing this oxidizing treatment, as shown in Fig. 1(d), spacers comprising oxide film 10, 10 are formed on the side walls of polysilicon layer and tungsten silicide layer, and on the gate oxide film. Incidentally, these spacers are used as a mask layer for forming an LDD (Lightly Doped Drain) structure, and as a protection layer for protecting the side walls of gate electrode.

In the heat treatment mentioned above, the atmosphere for performing heat treatment can include either oxygen or oxygen with moisture, because diffusion of oxidizing substance in the metallic silicide layer is restrained. Moreover, in order to obtain a preferable thickness of an oxide film, the atmosphere, process temperature, process time, gas flow quantity etc.

can be set voluntarily.

Fig. 2 shows a state of top surface of the gate electrode 5 formed by the manufacturing method of Embodiment 1. In Fig. 2, what is formed vertically in the central portion of the figure is the gate electrode 5. Moreover, what is formed at each side of the gate electrode 5 is the gate oxide film. As apparently shown in Fig. 2, abnormal oxidation resulting in deposition of notched crystal described referring to Fig. 5(b) does not come out on the side walls of gate electrode 5. That is, by the manufacturing method of present invention, the side wall of gate electrode is oxidized uniformly without any abnormal oxidization.

As described above, according to the manufacturing method of Embodiment 1, abnormal oxidation can be prevented when the side wall is oxidized after forming gate electrode, in any condition such as atmosphere (only oxygen or with moisture), process temperature, process time, gas flow quantity etc.

<Embodiment 2>

The manufacturing method of Embodiment 2 of present invention comprises a process of forming a gas electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat treatment of the metallic silicide layer at least a portion of which is exposed in an atmosphere consisting of a chief element of argon gas, and a process of forming spacers comprising oxide film on each side of the gate electrode; in this order.

The manufacturing method of Embodiment 2 is same as the manufacturing method of Embodiment 1 except the process of treating metallic silicide layer with heat; wherein the chief element of gas atmosphere for heat-treatment is not nitrogen, but argon.

That is, after forming a gate electrode 5 as well as the manufacturing method of Embodiment 1, heat-treatment in an atmosphere of chief element of argon gas is performed in a chamber of heat-treating apparatus (RTA) purged with argon gas. Here, chief element of argon gas means that the density of argon in the gas atmosphere is not less than 99%. And, especially, the density of oxidizable gas (oxygen gas etc.) is not more than 100 ppm.

In an atmosphere of chief element of argon gas, abnormal oxidation can be prevented as well as nitrogen gas. Moreover, a method by using argon gas of Embodiment 2 is profitable in the occasion when nitrization of source region or drain region of the semiconductor substrate must be avoided.

Incidentally, process temperature, process time etc. of heat-treatment condition is same as manufacturing method of Embodiment 1.

And, spacers comprising oxide film is formed on the side wall of gate electrode as same as Embodiment 1, after performing heat-treating process of metallic silicide layer, which is performed in the argon gas atmosphere of chief element.

<Embodiment 3>

The manufacturing method of Embodiment 3 comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat-treatment in an atmosphere of chief element of mixture gas consisting of nitrogen and ammonia, and a process of forming spacers comprising oxide film on the side wall of the gate electrode; in this order.

The method of Embodiment 3 is same as Embodiment 1 except the heat-treating process of metallic silicide layer, wherein the heat-treatment in a gas atmosphere of chief element is not nitrogen but mixture gas of nitrogen

and ammonia.

At first, a gate electrode 5 is formed as same as Embodiment 1. After this, a chamber is purged with nitrogen gas so as to make the density of oxidizable gas less than 100 ppm. Subsequently, the wafer is let in the chamber of heating apparatus so as to heat it with lamp.

In the meantime, the wafer is heated up to a prescribed temperature. Then, ammonia gas is introduced into the chamber. And, an atmosphere of mixture gas consisting of nitrogen and ammonia is made. Then, a heat-treatment is made. The temperature in this occasion is preferably not less than 650° C. And, it is still preferable if it is 700 to 800° C.

The density of ammonia gas in the atmosphere is preferable if it is 1 to 3% provided that the nitrified region mentioned later is formed in a reasonable range.

And, spacers comprising oxide film is formed on the side wall of gate electrode as same as Embodiment 1, after performing the heat-treating process of metallic silicide layer, which is performed in the atmosphere of mixture gas of chief elements of nitrogen and ammonia.

According to the method of Embodiment 3, abnormal oxidation on the side wall does not occur. And, as shown in Fig. 3, nitrified region 7 is formed in a range of side wall to the bottom portion of metallic silicide layer 3 assisted by the ammonia gas. Therefore, nitrogen of high density is introduced into the oxide film on the substrate except the portion under gate electrode 5. As a result, diffusion of impurities from the substrate to the spacers formed on the side wall of gate electrode 5 can be prevented.

After performing heat-treatment mentioned above, oxidizing treatment is performed in a common oxidizing furnace as same as Embodiment 1. The gas let in the furnace as an atmosphere in this occasion

preferably consists of a chief element of nitrogen. In the meantime, the furnace is heated up to a preferable temperature. Subsequently, a gas for oxidizing is introduced there.

This gas may consist of oxygen or moisture.

<Embodiment 4>

The method of Embodiment 4 of present invention comprises a process of forming a gate electrode having a metallic silicide layer on a semiconductor substrate, a process of performing heat-treatment of the metallic silicide layer at least a portion of which is exposed in an atmosphere of a chief element of nitrogen gas (heat-treating process of metallic silicide layer), and a process of forming spacers comprising oxide film on the side wall of gate electrode; in this order; wherein the heat-treating process of metallic silicide layer is performed after a process of performing reduced pressure treatment (reduced pressure treating process).

In the concrete, at first, etching for forming gate is performed as same as Embodiment 1. After etching for gate, the photoresist used for etching is removed. And, a gate electrode is formed. After this, the reduced pressure treating process is performed by using low pressure CVD device for example. Subsequently, a heat-treatment in an atmosphere of chief element of nitrogen gas is performed as same as Embodiment 1.

The reduced pressure treatment is performed by taking the semiconductor substrate formed the gate electrode in the furnace at its temperature of less than 550° C.

By performing the reduced pressure treatment, the density of oxygen on the surface of wafer (density of oxidizable gas) can be made less than 100 ppm.

After performing reduced pressure process, the wafer is heated up. And, heat treatment in atmosphere of a chief element of nitrogen gas at 700 to 800° C is performed as same as Embodiment 1 (heat treating process of metallic silicide layer).

In this occasion, if the wafer is heated up without performing reduced pressure process, abnormal oxidation occurs, because the density of oxygen between wafers is high.

The pressure of reduced pressure process is preferably 13 to 65Pa.

After performing heat treatment of more than 650° C, the wafer is cooled down to the process temperature or inletting temperature. Then, the wafer is taken out. After this, spacer comprising oxide film is formed on the side wall of gate electrode as same as Embodiment 1.

According to Embodiment 4, the density of oxidizable gas is efficiently decreased. Moreover, heat treating process of metallic silicide layer after reduced pressure process can be performed in processing apparatus, which can process a batch of wafers. Therefore, productivity can increase.

Next, an example of manufacturing method of NMOS-FET having LDD structure is described referring to Fig. 1 and Fig. 4.

At first, as mentioned before in the description with Fig. 1(a) to Fig. 1(c), gate electrode 5 (generally polysilicon) is formed on the semiconductor substrate 1. Next, as shown in Fig. 4(a), phosphorus is introduced by ion implantation using the gate electrode 5 as a mask. By this, shallow n^- layer 50 is formed all over the source and drain region of semiconductor substrate 1.

After this, as shown in Fig. 4(b), oxide film 10 (side wall) is formed on the side wall of gate electrode 5.

This oxide film 10 is formed with the condition mentioned before (condition described in Embodiments 1 to 4). By this, gate electrode with

restraining abnormal oxidation can be formed.

After forming oxide film 10, arsenic is introduced by ion implantation using oxide film 10 and gate electrode 5 as a mask. By this, deep n^+ layer 70 is formed in the portion of source and drain region distant from the gate electrode 5. After this, wiring etc. is performed. Then, NMOS-FET of LDD structure is manufactured.

Incidentally, the manufacturing method mentioned above is not only applied to NMOS-FET but also applied to various semiconductor elements such as CMOS-FET etc.

And, the present invention is not limited to Embodiments 1 to 4.

For example, the material of metallic silicide layer is not limited to Tungsten silicide, which is preferable in practical use. That is, molybdenum silicide or titanium silicide etc. is available.

Moreover, if the heat treatment after forming metallic silicide layer is performed at a temperature higher than the temperature of forming metallic silicide, SiN layer formed by reduced pressure CVD method is not always necessary.